

OPTIMIZATION OF THE DESIGN OF A WIDEBAND 1000 KV RESISTIVE REFERENCE DIVIDER

Alf-Peter Elg^{1*}, Jari Hällström² and Anders Bergman¹

¹SP Technical Research Institute of Sweden, SE-501 15 Borås, Sweden

²Centre for Metrology and Accreditation (MIKES), FI-02151 Espoo, Finland

*Email: <alf.elg@sp.se>

Abstract: The paper describes methods used for optimizing the design for a shielded resistive 1000 kV reference divider aimed primarily for d.c. calibration. Apart from having the utmost accuracy on d.c. voltage measurement, the divider is required to have a bandwidth of at least 10 kHz. Two designs have been modelled and compared, both consisting of 1000 reference resistors in series. The first design is a parallel RC divider; for this design ground capacitances affect the frequency response linearity. The second design is a shielded resistive divider where the parallel shielding branch is not physically connected to the purely resistive reference branch. Two methods for modelling the divider designs are described. Both analytical solutions of the circuits and circuit simulation software are used to obtain insight into the behaviour of the divider under design. The effects of capacitances to ground and between different stages of the dividers are included in the analysis, as well as inductance in the different branches of the studied topologies. The results show that with careful design the bandwidth of the 1000 kV divider under design can be in the range of tens of kilohertz, without compromising the precision of d.c. voltage measurement.

1 INTRODUCTION

Increasing transmission voltages in high voltage d.c. (HVDC) has accentuated the need for traceable calibrations of d.c. line voltage at levels above a few 100 kV. The application requires very good accuracy for d.c., but also good response to voltages with signal components up to a several kHz. Precision HVDC dividers are traditionally based on a resistive design, whereas high voltage a.c. (HVAC) dividers from 50 Hz and above typically rely on a capacitive or a transformer design. Owing to high resistance inherent in the d.c. dividers, switching from d.c. to even VLF a.c. will usually produce problems related to stray capacitances.

The complexity of a hybrid divider, composed of both resistors and reactive components, rapidly grows as the number of components increase, and a frequency response becomes hard to predict without recourse to detailed analysis.

In fact the experience from impulse voltage reference divider design can be applied also to wideband d.c. dividers. One resistive LI divider approach is based on non-linear high voltage resistance distribution [1],[2] and the other on field grading using additional electrodes [3]-[5]. The latter approach is chosen for more detailed study in this paper. Field grading has been used to extend the frequency range also on some earlier designs of reference d.c. dividers [6], but not on 1000 kV level [7].

Two approaches have been applied to model frequency and time response of a divider. The first approach is a computer program running the analytical solution for a specific divider topology. The other approach combines results from electric field simulations with traditional circuit simulator.

Measurements on existing resistive dividers have been performed and the results are used for verifying the models. Two dividers have been studied. A 200 kV precision resistive divider with wire-wound resistors that represents a typical unshielded reference divider design, and a prototype shielded divider with metal film resistors, built to test the simulation results.

The goal of this work is to optimize and build a divider for 1000 kV, having a wide bandwidth without compromising d.c. accuracy. To minimize self-heating effects, a low nominal current, 100 μ A, was chosen this design. This moves the design challenges to master leakage current and dielectric absorption effects on the insulation structures.

The 1000 kV divider is sectioned in 200 kV modules. These modules may also be used separately as 200 kV dividers. The 200 kV modules are also sectioned in smaller, e.g. 25 kV, modules, which will be referred to as sub-modules for the 1000 kV divider.

2 STUDIED TOPOLOGIES

Studied divider topologies, parallel RC and shielded resistive, are based on a series connection of one thousand 10 M Ω resistors. The

models assume that the divider consists of five 200 kV modules with intermediate external field grading electrodes.

2.1 Parallel RC divider

First approximation of the model used for a parallel RC divider is shown in Figure 1. The stray capacitances of the high voltage arm are not shown. In more detailed model each resistor is modelled as a resistance in series with an inductance. To reach proper wide band response the time constants in the high and low voltage arms have to be matched.

The drawback of this design is the parallel capacitor. Even the best capacitors available will be prone to problems with polarization currents, which can lead to long settling time.

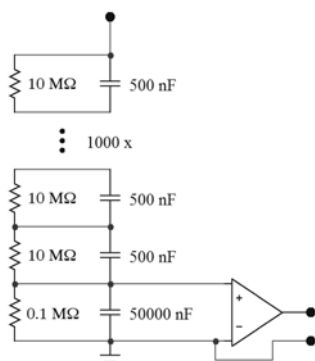


Figure 1: Simplified parallel RC divider model with approximate component values.

2.2 Shielded resistive divider

The model used for shielded resistive design consists of two parallel RC chains. The reference resistor branch is modelled with a small parallel capacitance for each resistor, whereas the shielding branch (surrounding the reference branch) is capacitive, with high valued discharge resistors in parallel. Figure 2 shows the model. For simplicity stray capacitances, apart from that in parallel with the reference branch resistors, are not shown.

A number of stray capacitances, e.g. between the external shields and between the shields and ground, have to be taken into consideration in the optimization of the design.

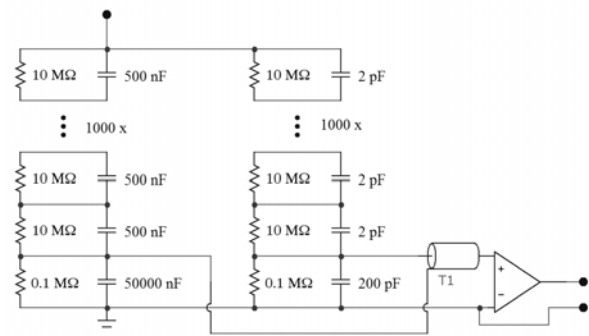


Figure 2: Simplified shielded resistive divider model with approximate component values. Shielding branch components are shown on the left.

The advantage of this design is that no compromise with d.c. response is required. The insulation for the reference branch can be designed as for a pure d.c. divider. However the more complicated topology leads to more complicated mechanical structure; also care has to be exercised to properly balance the two low voltage arms.

3 SIMULATION METHODS

The analytical formulae describing the circuits can be implemented in custom software to create an efficient tool to study the effect of variation of the parameters of the circuit. The drawback is that the analytical formulae are not always straightforward to derive, as for example, the case of the shielded resistive divider topology.

To be able to study the behaviour of the shielded resistive divider, too, we chose a solution, where the stray capacitances were obtained by field simulation software, and then fed into a circuit simulator. The advantage is that the complexity of the circuit is not limited, and the drawback is the longer time required for recalculation with new input parameters.

3.1 Analytical solution

To obtain the analytical solution for the circuit shown in Figure 1, we derive the impedance Z_i for the low voltage stage of the divider for a frequency range. The impedance Z_i of each sub-module is then calculated to estimate Z at each level in the stack, taking stray capacitance to earth $C_{i,e}$, from the local position of the stack into account. This calculation is repeated for each sub-module of the divider in an iterative process. The software permits to interactively change the values of the components, while observing the frequency response, which is plotted as amplitude and phase response as functions of frequency and position along the stack.

We now apply this method and model a case similar to the one in **Figure 1**, where we have a 200 kV divider consisting of 8 sub-modules. Here Z_1 is $2.002 \text{ M}\Omega // 3.9 \text{ nF}$, each sub-module Z_i is $10 \text{ M}\Omega // 22 \text{ pF}$, and from every sub-module we have a stray capacitance of 0.6 pF to earth. The dividing factor is 1000. The result showed in **Figure 3**, shows the voltage quotient U/U_{ref} and the phase as function of frequency, where U_{ref} corresponds to a linear distribution.

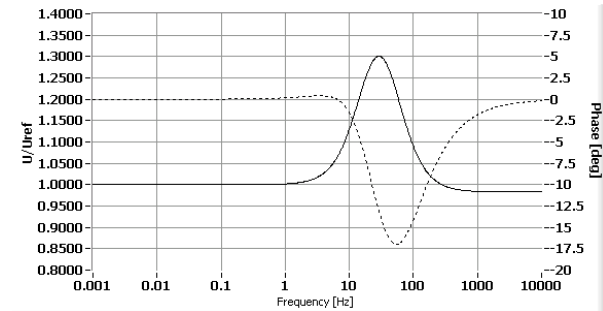


Figure 3: Divider response. Solid line: amplitude response, dashed line: phase response.

Since we know the impedance at each level in the divider we may now observe the amplitude response as a function of location in a 200 kV module and frequency. **Figure 4** shows the voltage quota as a function of position in the stack of 8 submodules.

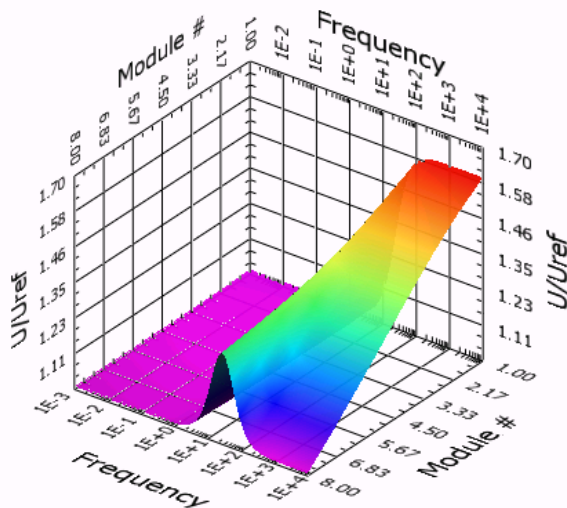


Figure 4: Ratio between the modelled and ideal voltage distributions of a 200 kV module as a function of position in the module and frequency. U_{ref} responds to linear voltage distribution.

For low frequencies in **Figure 4**, approaching d.c. conditions, we have response close to ideal. From 10 Hz the response is influenced by the non-uniform stray capacitance, even though the divider is balanced with a capacitance in the low voltage arm.

3.2 Combining field and circuit simulations

The optimization process performed for the shielded resistive divider starts from the mechanical and dielectric structure of the divider. After the position and dimensions of the shielding electrodes are set, the electric field distribution can be modelled using finite element method (FEM). An example is shown in **Figure 5**, where the voltages of the external electrodes are set to 200, 400, 600, 800 and 1000 kV. The goal is to have a linear field distribution along the resistive column.

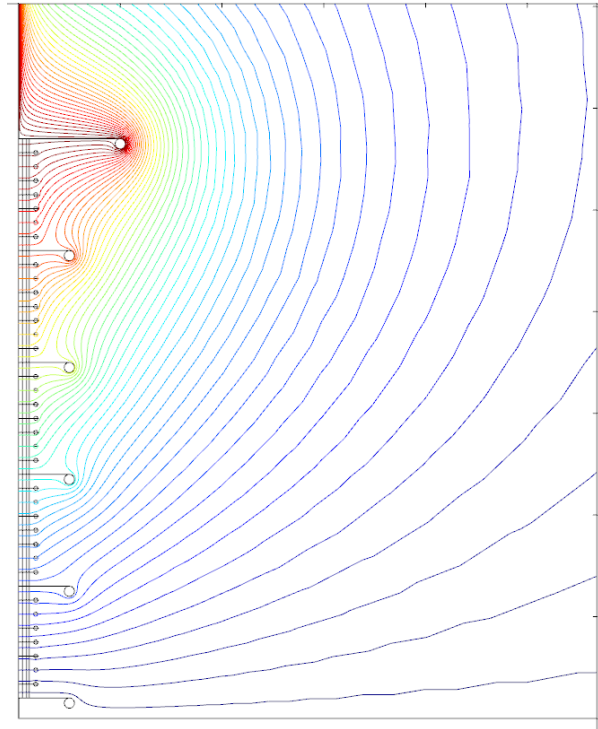


Figure 5: Divider equipotential lines for a linear field distribution along reference resistor position.

The next step in the process is to use the FEM software to solve all stray capacitances between all external electrodes and internal electrodes, and ground. In our example the total number of electrode nodes is 6, leading to 15 capacitance values. In the more detailed model the number of free nodes has been up to 43, leading to 903 solved stray capacitance values. Fortunately most of these are very small and can be neglected. In the detailed model only the capacitances between the external electrodes and capacitances internal to each module are added to the simplified model shown in **Figure 2**.

The final step is to let the circuit simulation software tune the 500 nF capacitor in the shielding branch to produce 200, 400, 600, 800 and 1000 kV onto the external electrodes also on higher frequencies.

An example of optimization result, showing the order of magnitude for the tuning, is shown in Table 1. The starting point for the optimization was 1100 pF total capacitance for each 200 kV module, and the outcome was that to compensate for the stray capacitances this value should be tuned upwards from 30 to 270 pF (about 3 % to 25 %), depending on the position in the stack.

Table 1: Example of solved stray capacitances between the external electrodes (top right), and the grading capacitor values required to reach linear capacitive voltage distribution. (bottom left).

		Stray capacitances per 200 kV unit [pF]					
		Gnd	20 %	40 %	60 %	80 %	100 %
Shield grading capacitors per 200 kV unit.	Gnd		65	40	33	22	46
	20 %	1100		17	3.9	1.3	1.7
	40 %		1100 + 31		19	3.9	4.2
	60 %			1100 + 87		16	10
	80 %				1100 + 177		25
	100 %					1100 + 268	
	Nominal + optimization [pF]						

Due to its relatively high capacitance the shielding branch will now have a linear voltage distribution, both for d.c. and a.c.. The reference branch resistors, located within the shielding branch, will have a good a.c. response, too, as stray capacitance is compensated by the strong shielding branch.

4 DESIGN DETAILS

4.1 Electrode shapes

The next step is to look at the shape of the electrodes. An example is given of how the shape of a corona shield may influence the stray capacitances. In Figure 6 we have an example of a slightly folded shield which gives larger radial components, hence stray capacitance, than the straight shields in Figure 7.

4.2 Low voltage arm

In the low voltage arm, stray effects can be considered negligible, and accuracy sufficient for this application can be reached by using lumped constant analysis of the circuit, based on component values. The values of resistors and capacitors will have to be adjusted to achieve the same voltage ratio for both divider chains and both for resistive and capacitive branches.

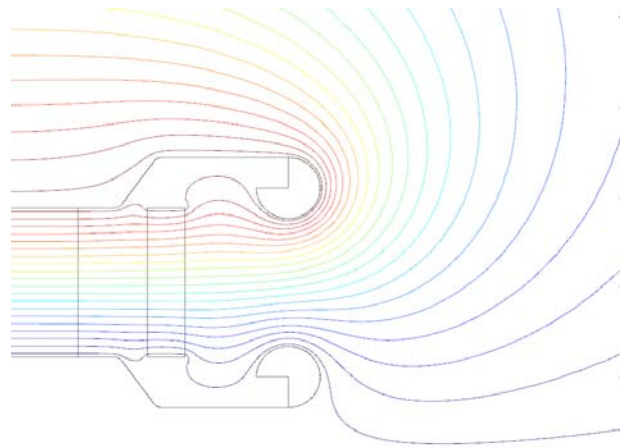


Figure 6: Folded corona shields with equipotential lines.

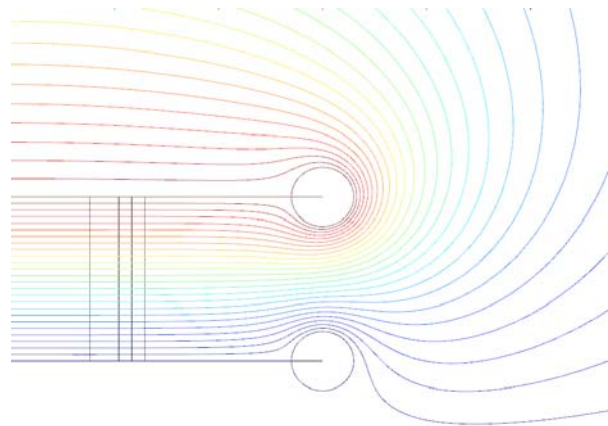


Figure 7: Straight corona shields with equipotential lines.

5 CASE STUDIES

The results of the simulations are verified against measured performance of both a purely resistive 200 kV divider, and a low voltage prototype of a shielded resistive divider.

5.1 Pure resistive divider

The divider is capable of a precision in the 10 ppm range for d.c., but shows large deviations of more than 20 % for a.c. in the range 0.1 Hz – 1 kHz. Apparently stray capacitances come into play. The result of comparison of modelling with the measured frequency response is given in Figure 8. The 200 kV divider consists of 200 resistors of 10 MΩ. Stray capacitances to earth are estimated to 0.6 pF per 25 kV submodule and the capacitance parallel to the divider resistors is about 22 pF per 25 kV submodule. The low voltage arm is balanced by 3.9 nF. We have a good correlation in amplitude between the model and the data, but the phase prediction is not as good.

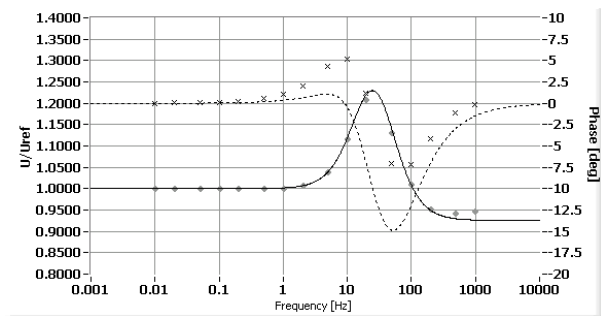


Figure 8: Simulation (lines) compared with measured response (dots), resistive divider. Solid line: amplitude response, dashed line: phase response.

5.2 Parallel RC divider

The pure resistive divider was modified adding a 1 nF capacitance in parallel to each 25 kV submodule of the precision stack of resistors. The intention was to study whether the frequency response up to 10 kHz could be improved. The resonance peak amplitude goes down to about 0.5 % from 25 %, and the resonance moves down in frequency by more than one decade as shown in Figure 9. We also see that the model does not this time take all effects into account in detail, as the match between simulation and measurement we had in Figure 8 is lost.

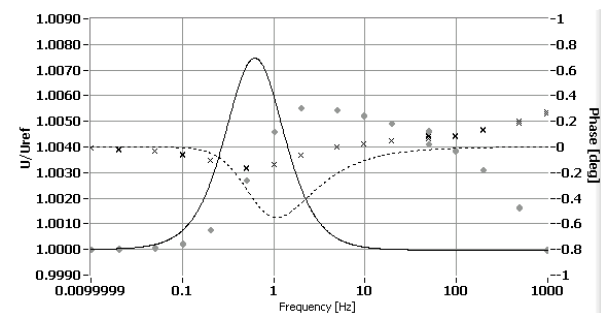


Figure 9: As Figure 9, but with increased parallel capacitance. Solid line: amplitude response, dashed line: phase response.

5.3 Shielded resistive divider

In the third example we have built a prototype of a shielded divider. This divider was built on the principle of the divider in Figure 2 with 8 modules. Around a centre column of PMMA tube 1 M Ω resistors, 50 per module, were mounted in series for the precision stack, also with the possibility to add a single capacitor in parallel. The shield consisted of 25 pieces of 47 nF capacitors, each in parallel with a 10 M Ω bleeder resistor for d.c. measurements. The time constant on the low voltage arm was balanced both in the precision stack and the shield stack. It is important to keep the floating precision stack at the same potential as the shield, especially close to the shield electrodes,

to avoid capacitive coupling and electric breakdown.

This divider has given much experience in both the choice of combinations of components but most of all the geometrical design. One of the most important observations was that unwanted stray capacitances can easily be built in by wrong choices of geometries, which was also confirmed by modelling with field simulator. In Figure 11 we show the combination of a measurement, and circuit simulator response based on field simulations. The deviation from d.c. ratio has now lowered to 0.04 % compared to c. 5 % of the parallel RC divider (Figure 10).

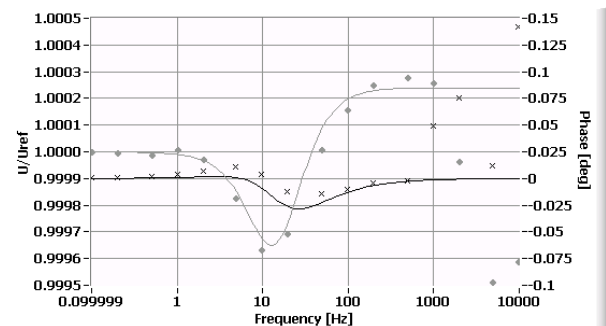


Figure 10: Simulation (lines) compared with measured response (dots), shielded resistive divider. Solid line: amplitude response, dashed line: phase response.

6 CONCLUSIONS

We have presented two methods for modelling a divider design. Both analytical solutions of the circuits and circuit simulation software combined with field simulations have given insight into the behaviour of the divider under design. The results show that with careful design the bandwidth of the 1000 kV divider under design can be in the range of tens of kilohertz, without compromising the precision of d.c. voltage measurement.

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