DESIGN OF A HYBRID MATRIX FAULT CURRENT LIMITER USING LOW-POWER PTC RESISTORS AND FAST SWITCHES FOR MEDIUM VOLTAGE

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Abstract: This paper presents a hybrid matrix fault current limiter using fast switches to reduce loss of the PTC device. The PTC matrix consists of a parallel-series (matrix) combination of PTC resistors. In this approach, during normal operation, the fast switch has to carry the load current so the PTC matrix has no effect in normal operation and there is no resistive loss. When a fault occurs, the fast switch commutates the fault current onto the PTC matrix. When the current flowing through the PTC matrix exceeds the current limit, the PTC resistors warm up above a threshold temperature and the electrical resistance of the PTC matrix suddenly increases several orders of magnitude to a tripped state where the resistance will typically be hundreds or thousands of ohms, greatly reducing the current. Arc voltage plays a great role in commutation process. In this paper arc model for fast switches is considered for calculations. The arc model is based on the combination of Mayr and Cassie arc models. To commutate the instant current onto the PTC matrix, the arc voltage must be high enough (almost 1kV). A number of breakers in series, driven by one drive are used to obtain high arc voltage.

1 INTRODUCTION

With networks connection to each other, short circuit current level is rising. Ways of limiting this current have a great impact on equipment design, maintenance and power quality. Until now, different technologies have been used for current limitation. One of these technologies is using the PTC effect for current limitation [1-3]. When the current flowing through a PTC resistor exceeds the current limit, the PTC resistor warms up above a threshold temperature and its resistance suddenly increases several orders of magnitude to a tripped state where the resistance will typically be hundreds or thousands of ohms, greatly reducing the current. This allows the use of a cheap and simple circuit breaker in series with the PTC resistor to disconnect the circuit.

Combining several PTC resistors is a means to increase performance [4-6], such as the extension to higher rated currents and higher rated voltages, and reduce cost in FCL. For extending this concept parallel-series (matrix) combination of low-power PTC resistors is considered.

There are two important factors which determine the operation of a PTC matrix, namely, statistical variations of the properties of the PTC resistors and thermal interaction of the PTC resistors.

This paper presents a hybrid matrix fault current limiter using fast switches. In this approach, during normal operation, the fast switch has to carry the load current so the PTC matrix has no effect in normal operation and there is no resistive loss. When a fault occurs, the fast switch commutates the fault current onto the PTC matrix and the current limitation begins.

2 PTC MATRIX OPERATION

2.1 Normal operation

Although in the presented approach the PTC matrix has no effect in normal operation, a short look at its normal operation might be useful for understanding the benefits of the hybrid fault current limiter.

Rated current, cold resistance of the PTC resistors and efficiency of heat transfer to the environment are important figures that play a great role in design of a PTC matrix in its normal operation.

The heat transfer characteristics of a single PTC resistor can be expressed by a heat transfer coefficient H, which relates the rate of heat generation $R_C I_r^2$ in the PTC resistor to its over-temperature T_S-T_A with respect to the environment:

$$R_C I_r^2 = HA(T_S - T_A) \qquad (1)$$

Where: R_C = PTC cold resistance in (Ω)
I_r = rated current of the PTC resistor in (A)
A = heat transfer surface in (m^2)
T_S = surface temperature of the PTC Resistor in (K)
T_A = the ambient temperature in (K)

In a PTC matrix in addition to heat transfer by convection, some thermal energy is transferred by conduction between matrix elements. Figure 1 shows the heat transfer structure of a matrix in terms of the thermal conduction resistances R

connecting an element to its neighbours and to the environment. R_{ij}^{t1} , R_{ij}^{t2} are the thermal resistances to neighbouring elements parallel and in series and R_{ij}^{amb} is the thermal resistance towards the environment.

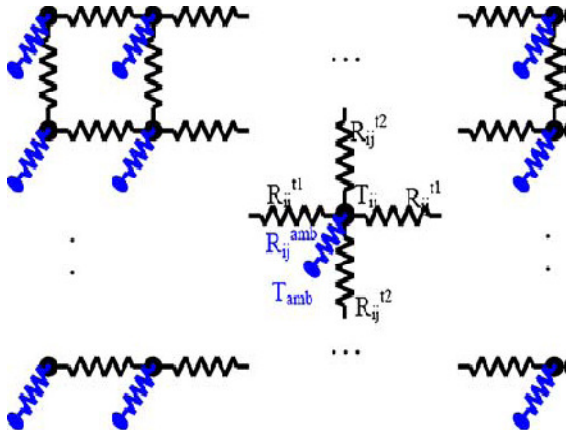

Figure 1: Heat transfer network for the calculation of operating temperatures of PTC resistors [5]

2.2 Limiting operation

The critical issue under limiting operation is statistical variation of the properties of the PTC resistors especially PTC cold resistance. This variation can be as high as %25 [7]. It seems that this variation can cause a problem for current distribution, but simulation results showes that current distribution is uniform in the PTC matrix. In fact, flowing a higher current through a PTC resistor warms it up and increases its resistance so the current has to flow through the branches with less resistance.

Voltage distribution in a PTC matrix is another problem that is caused by resistance variation [4]. During a fault condition, one of the PTC resistors interrupts first and its resistance increases rapidly. Therefore the voltage between two ends of this PTC resistor reaches almost applied voltage. Since a single PTC resistor is not able to hold the applied high voltage, breakdown occurs in this PTC resistor and respectively in other PTC resistors. This problem is solved by using varistors in parallel with PTC resistors.

3 BLACK BOX ARC MODELING

3.1 Background

Black box arc models describe the dynamic behavior of the arc in an integral form. They are used to predict the interruption capabilities of circuit breakers under certain test conditions. Some of these models are described in [8].

The fundamental concept of arc modeling is based on the energy balance between heat production inside the arc and the cooling power. Therefore the conductance g of the arc is a function of its heat content Q by the following differential equation [9]:

$$\frac{dg}{dt} = \frac{dg}{dQ}(P_{in} - P_{out}) \qquad (2)$$

Where: P_{in} = heating power in (W)
P_{out} = cooling power in (W)

Almost all arc models can be described by the following equation [8]:

$$\frac{1}{g}\frac{dg}{dt} = \frac{1}{\tau(t)}\left(\frac{ui}{P(t)} - 1\right) \qquad (3)$$

The heating power is assumed to be equal to the electric power ui. The cooling power P and the thermal damping $1/\tau$ are in general assumed to be time dependent. In special cases P and τ can be found as functions of the current i, the conductance g or the heating power ui.

Several combinations of the Mayr and Cassie equations were introduced to extend the area of validity. For example in [10] it is proposed to combine the Mayr and Cassie equations by using a current dependent weighting function in order to ensure a smooth transition between the two models.

3.2 Arc modelling in fast switches

As mentioned above, to investigate the current commutation, the arc model for fast switches is needed. Therefore in this section main parameters for rapidly elongated arcs is described.

The arc voltage is divided in to two parts: the electrode region and the arc column voltage drop. The electrode region includes the anode and the cathode region. The overall conductivity can be written as:

$$\frac{1}{g} = \frac{1}{g_E} + \frac{1}{g_c} \qquad (4)$$

Where: g_E = electrode region conductance in (S)
g_c = arc column conductance in (S)

Voltage drop near the electrodes or U_E is to a large extent independent of the arc current. This voltage drop occurs instantaneously after opening the fast switch. So the value of U_E has a great impact on current commutation at the beginning of the commutation process. The value of U_E is approximately 17 V [9].

Both, the Cassie and the Mayr equations are widely used to model the dynamic behavior of the arc. However, the Mayr equation is a better

description for lower currents while the Cassie equation is a better description in the high current range.

In a hybrid FCL, the value of arc current falls from a high level to zero after arc extinction in a few 100 microseconds. Therefore the combination of Mayr and Cassie models is used for arc modelling. In [10] it is proposed to combine the Mayr and Cassie equations by using a current dependent weighting function. This model is described by the following equation:

$$\frac{1}{g_c}\frac{dg_c}{dt}=\frac{1}{\tau(t)}\left((1-\sigma)\frac{u_c i_s}{u_0^2(t)g_c}+\sigma\frac{u_c i_s}{P_m(t)}-1\right) \quad (5)$$

In this equation the heating power is equal to $u_c i_s$. σ is weighting function and its value varies from zero to one. The Cassie-part is described by the arc parameter u_0^2 and the Mayr-part is described by the arc parameter P_m.

Since the cooling power of the arc largely depends on the arc length, u_0^2 and P_m are functions of the arc length. The thermal damping is assumed to be function of arc current. So the (5) can be written as following [9]:

$$\frac{1}{g_c}\frac{dg_c}{dt}=\frac{1}{\tau(|i_s|)}\left((1-\sigma)\frac{u_c i_s}{u_0^2(x)g_c}+\sigma\frac{u_c i_s}{P_m(x)}-1\right) \quad (6)$$

A definition of the weighting function is described as [10]:

$$\sigma=\exp(-\frac{i_s^2}{I_T^2}) \quad (7)$$

Where: i_s = arc current in (A)
I_T = transition current in (A)

The transition current is limit of the validity of the Cassie arc models and is equal to 150 A.

The Cassie parameter u_0^2 increases proportionally to the arc length in high arc currents [9]. So the following equation is used to describe the relation between the Cassie parameter and the arc length [9]:

$$u_0^2(x)=b.x \quad (8)$$

The arc parameter b is then constant in the high current range. Its value is about 10^5 V^2/m.

In the low current range the arc column becomes unstable. So there is no specific relation between the cooling power of the arc column and the arc length. Therefore, the heat loss is defined to remain constant at the level of the heat loss of the Cassie equation at the transition current I_T (150 A) [9].

The time constant τ is defined to increase with regard to the equation that has been proposed in [8]:

$$\tau=\tau_0+\tau_1\exp(-3\frac{|i_s|}{I_T}) \quad (9)$$

In this equation τ_0 = 1 µs and τ_1 = 40 µs.

4 DESIGN AND SIMULATION RESULTS

4.1 Equivalent circuit

In this section a hybrid fault current limiter is designed for a 12kV single phase network. The PTC matrix must interrupt a fault current with symmetrical peak current of 20 kA. However, in the first cycle the value of fault current reaches almost 35 kA. Figure 2 shows the equivalent circuit of a hybrid FCL.

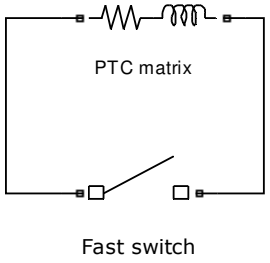

Figure 2: The equivalent circuit of a hybrid FCL

The hybrid FCL consists of a fast switch and a parallel path with a PTC matrix. In this circuit when a fault occurs, the fast switch opens in a few 100 microseconds and the fault current commutes from the fast switch to the parallel path. The opening speed of the fast switch is regarded to be almost 20 m/s. A high speed repulsion drive can provide an extremely short breaking time [11].

Arc voltage plays a great role in commutation process. To commutate the instant current onto the PTC matrix, the arc voltage must be high enough. Since in a single breaker, the arc voltage reaches a maximum of about 40-50 V, a series of breaks are needed to obtain high enough voltage. In this design fast switch has 20 breaks in series and the resultant arc voltage is almost 1000 V after a few 100 microseconds. It is assumed that the fault current is commutated on to the PTC matrix before it reaches 5 kA.

For a complete current commutation the following condition must be established:

$$\frac{u_s}{R_{C\max}} > I_{ins} \qquad (10)$$

Where: u_s = arc voltage in (V)
R_{Cmax} = maximum value of the PTC cold resistance in (Ω)
I_{ins} = instantaneous current in (A)

Since the arc voltage reaches almost 1000 V, the maximum value of the PTC matrix cold resistance must be 0.2Ω.

4.2 Low-power PTC resistor

The PTC matrix consists of a number of low-power PTC resistors. Siemens C915 is used as low-power PTC resistor. According to the resistance versus temperature characteristic of Siemens C915 [7], the critical temperature is 120 °C and the value of cold resistance is almost 0.2Ω. The value of cold resistance has tolerance of ±25% [7]. Therefore for accurate simulation, the normal distribution is used for this value.

Calculation the number of PTC resistors is first step in the PTC matrix design. We only consider the simplest case, in which the matrix consists of a series combination of ***n*** elements, each consisting of ***m*** elements connected in parallel.

Number of ***n*** dimensions of the PTC matrix is determined by breakdown voltage of the PTC resistors. The experimental results showed that the breakdown voltage of the PTC resistors is almost 1kV. In a single phase 12 kV network the peak voltage is 17kV. During fault current limitation the resistance of the PTC matrix increases several orders of magnitude, so the voltage of the matrix reaches to applied voltage. Therefore the value of ***n*** or number of series element must be at least 17.

Number of ***m*** dimensions is determined by the value of R_{Cmax}. To obtain maximum value of 0.2Ω for R_{Cmax} number of parallel element must be at least 17.

4.3 Simulation results

When triggered by an external fault detection system, the fast switch has to commutate the instant current onto the parallel path at 1.8 ms. The overall arc voltage is the total sum of the individual arc voltages of the series breaks.

As shown in the figure 3, after opening the fast switch at 1.8 ms, the fault current commutates to the PTC matrix in almost 300 µs. The overall fault current flows entirely through the PTC matrix and heats the low-power PTC resistors which intern increases its resistance and finally at t = 5.6 ms the fault current is limited.

The PTC voltage is shown in the figure 4. It can be seen that the U_E occurs instantaneously after opening the fast switch. The U_E is sum of electrode region voltage drop of 20 breaks. Therefore the voltage of the PTC matrix is 340 V at t = 1.8 ms.

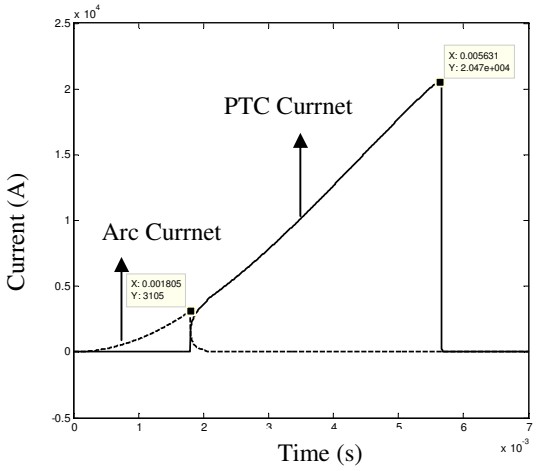

Figure 3: The commutation process of fault current

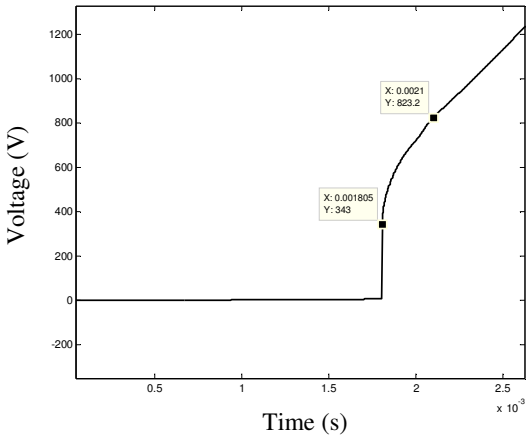

Figure 4: The voltage drop of the PTC matrix

By increasing the speed of repulsion drive the fault current commutates faster on to the PTC matrix. Figure 5 shows the effect of opening speed on the commutation process.

5 CONCLUSION

This paper presents some basic considerations to evaluate the potential of upgrading the performance of a fault current limiter by parallel-series (matrix) combination of low-power PTC resistors. Since the rated current of low-power PTC resistors is almost 3 A, flowing the high currents need a lot of parallel branches and a strong cooling mechanism. On the other hand the resistive loss of such a current limiter can be so high.

In this approach, during normal operation, the fast switch has to carry the load current so the PTC matrix has no effect in normal operation and there is no resistive loss. Also the cooling method of PTC matrix can be very simple.

The presented approach showed that in each switch, the arc extinguishes without means of forced arc cooling within a few 100 microseconds.

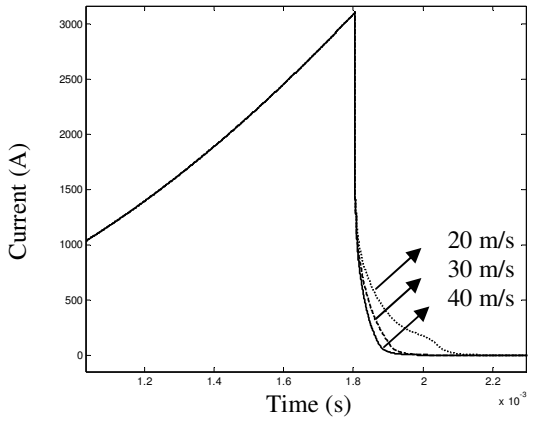

Figure 5: Effect of opening speed on current commutation

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