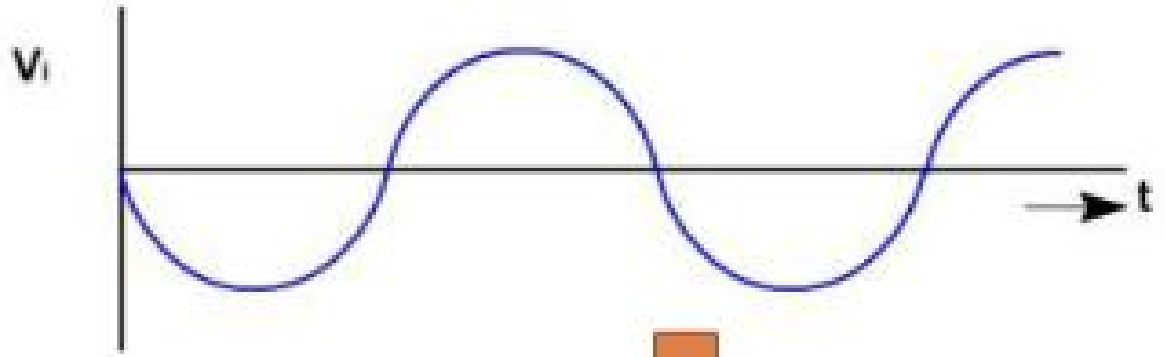
ANALOG PULSE AND SWITCHING LAB

Diode Applications : Clampers

Objectives

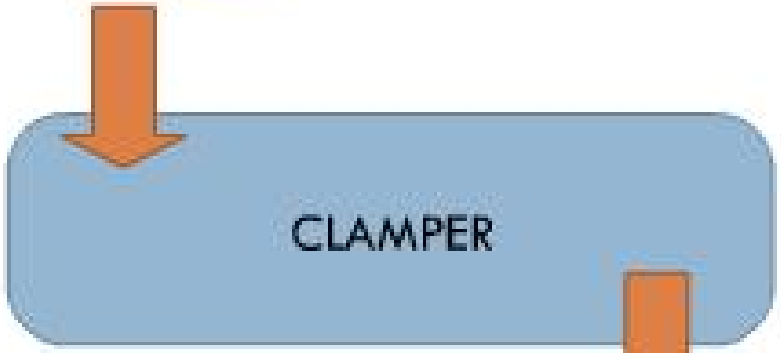
- Learn about clamper circuits
- Positive Clamper
- Negative Clamper
- Biased Positive Clamper
- Biased Negative Clamper

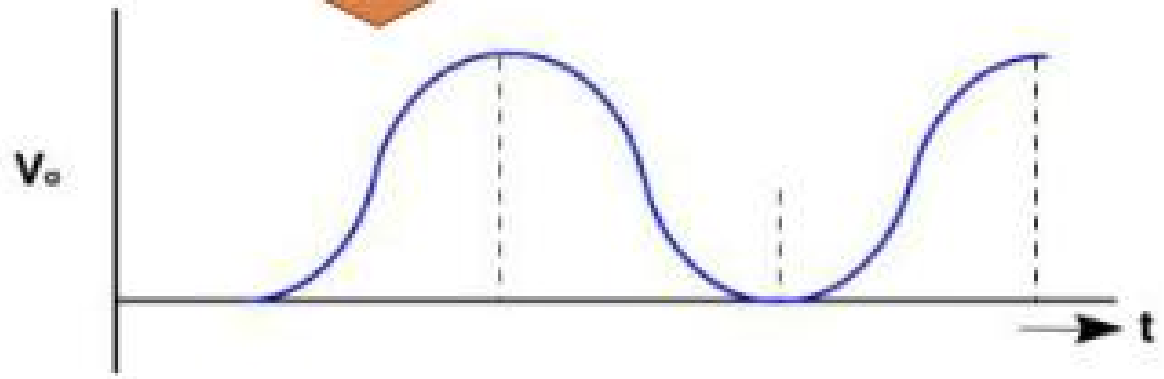
What are Clampers ?



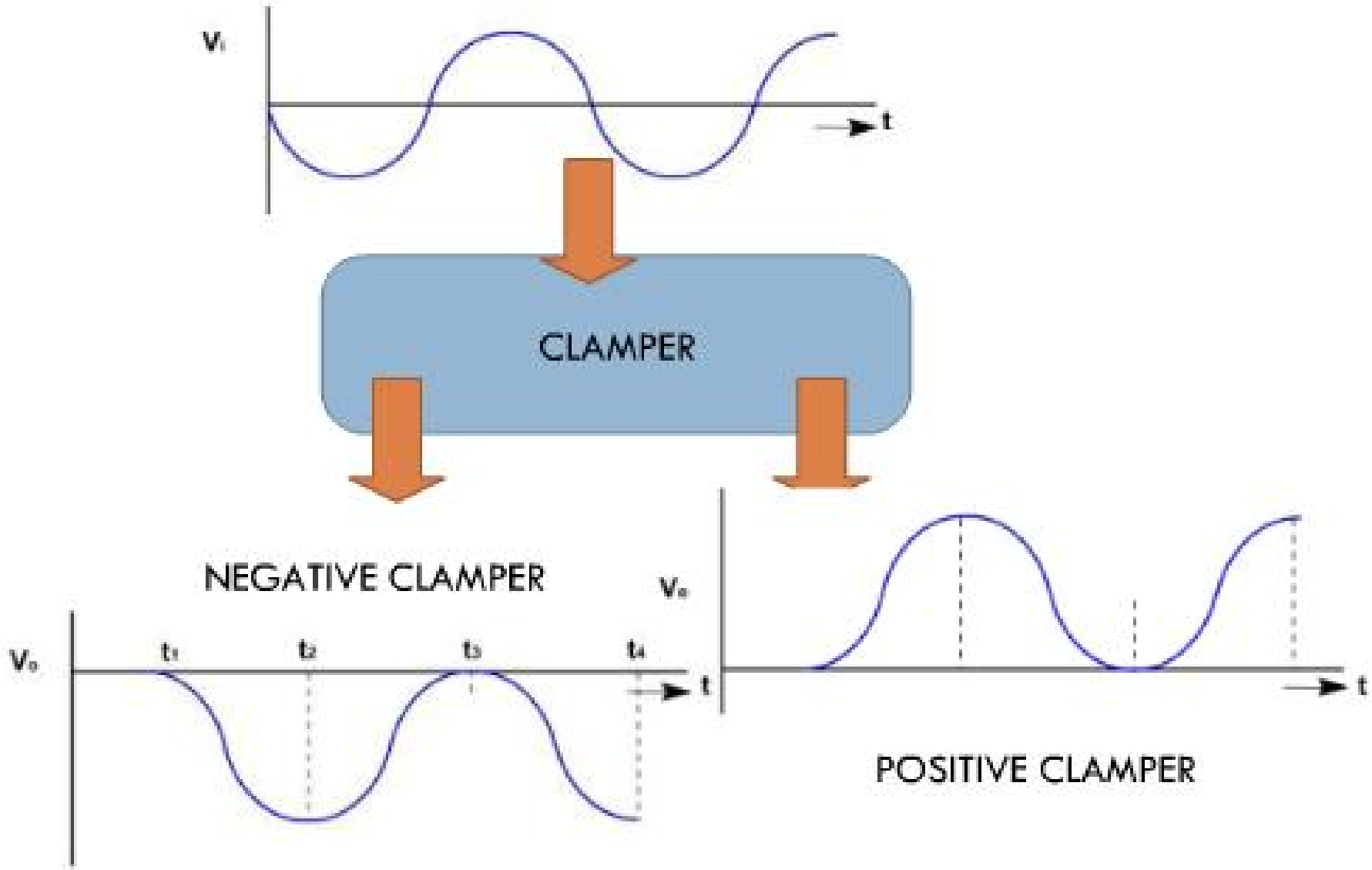
Clampers are also known as **dc restorers** or **clamped capacitors.**

Clampers shift an input signal by an amount defined by an independent voltage source.



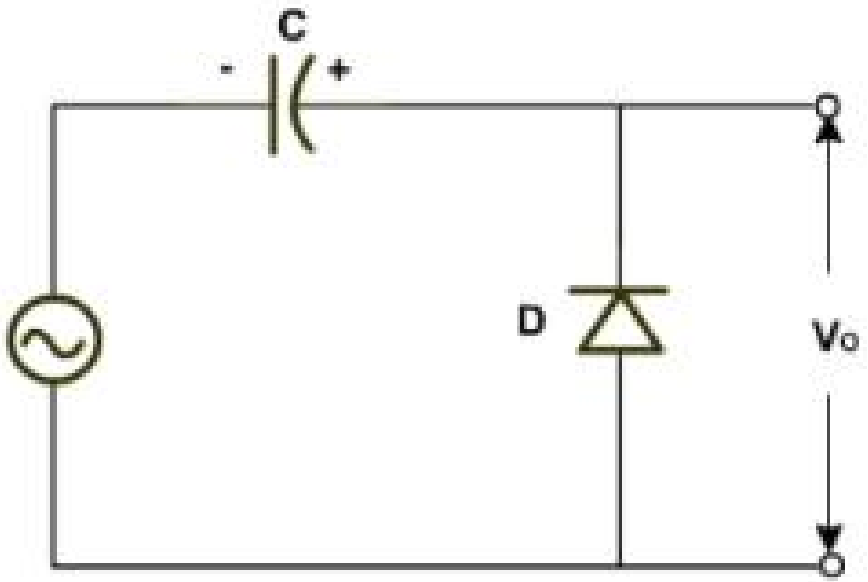


Types of Clampers ?



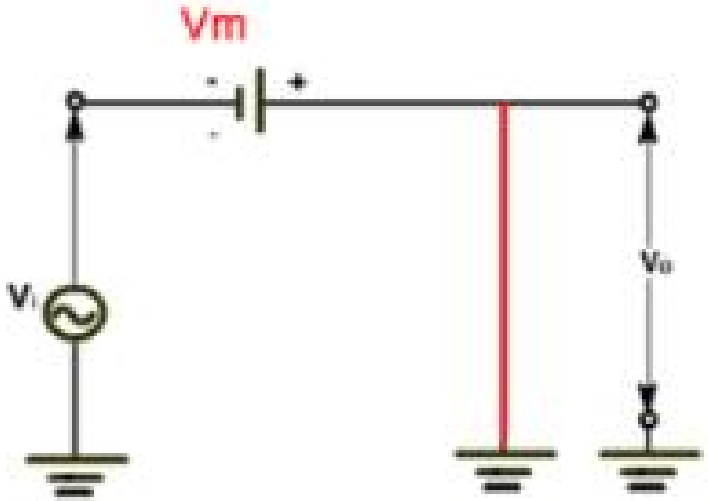
Positive Clamper

Positive clamping circuit clamps the input signal to the +ve Dc level i.e. above the zero level.



Positive Clamper : -ve Half Cycle

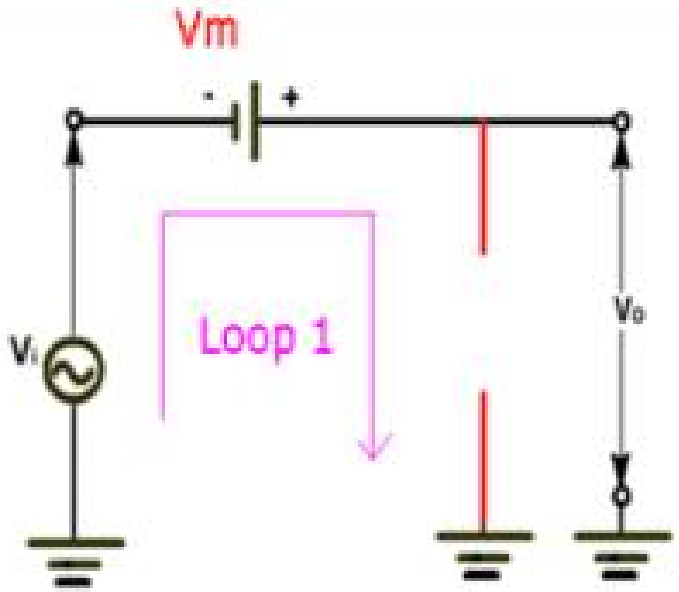
During the negative half cycle of the inputsignal,diode is forward biased, thus conducts and acts like a short circuit. The output voltage $V_o \Rightarrow 0$ volts. The capacitor is charged to the peak value of input voltage V_m. and it behaves like a battery (DC source of magnitude Vm).



During the -ve cycle diode turns on

Positive Clamper : +ve Half Cycle

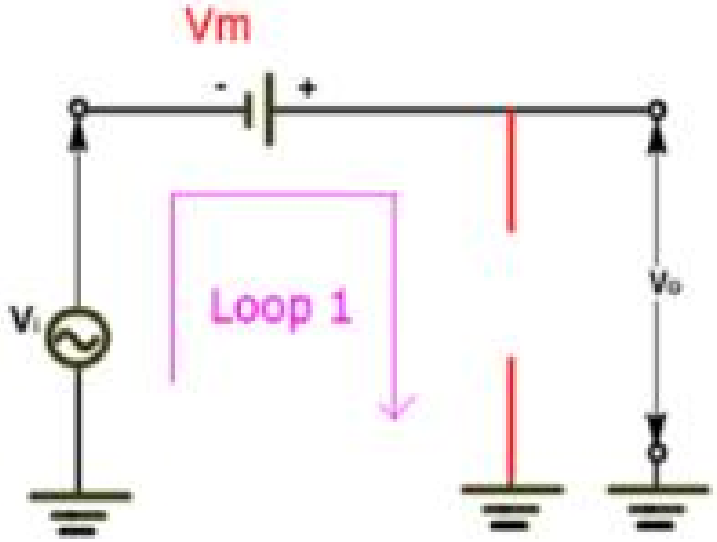
During the positive half of the input signal, the diode does not conduct and acts as an open circuit. Capacitor can only discharge through the R(Load). Since RL has high resistance, the capacitor discharges very little each period.



During the + ve cycle diode turns off

Positive Clamper – Circuit Analysis

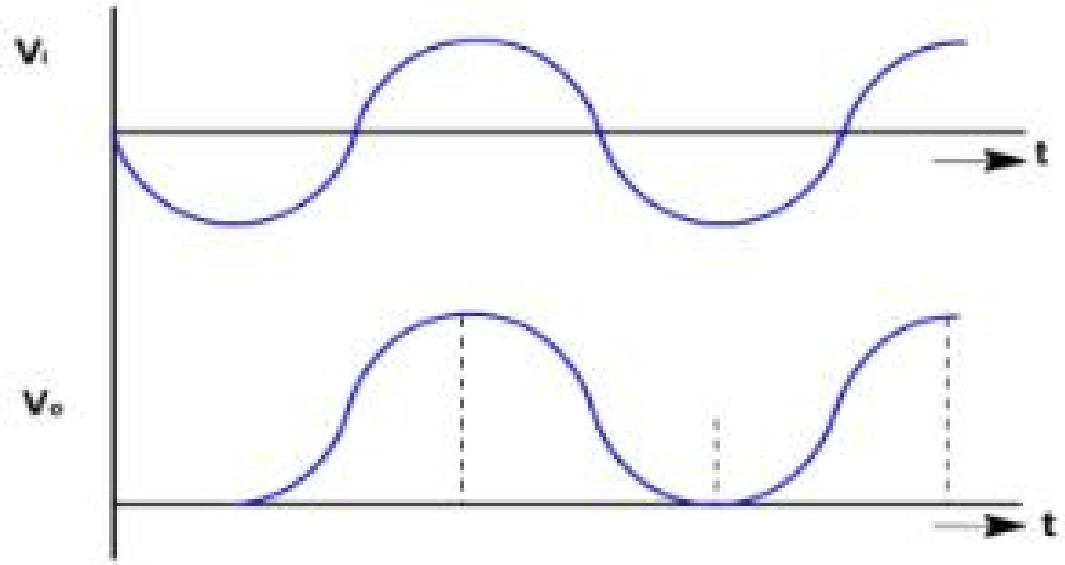
Applying KVL across loop 1(KVL at maximum positive input, $v_{in}=+V_m$), Vi + Vm – Vout =0 Hence the output voltage, $V_{out} \Rightarrow$ Vin (peak)+ $V_m = V_m + V_m$. This gives a positively clamped voltage. $V_o \Rightarrow V_m + V_m = 2\,V_m$



During the + ve cycle diode turns off

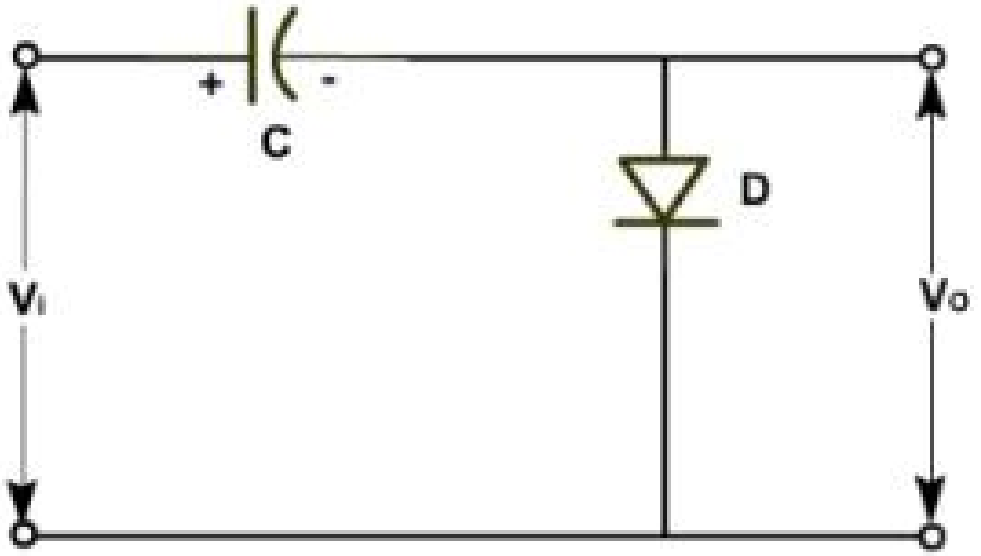
Positive Clamper – Waveform

A diode clamper adds a DC level to an AC voltage. The capacitor charges to the peak of the supply minus the diode drop. Once charged, the capacitor acts like a battery in series with the input voltage. The AC voltage will "ride" along with the DC voltage. The polarity arrangement of the diode determines whether the DC voltage is negative or positive.



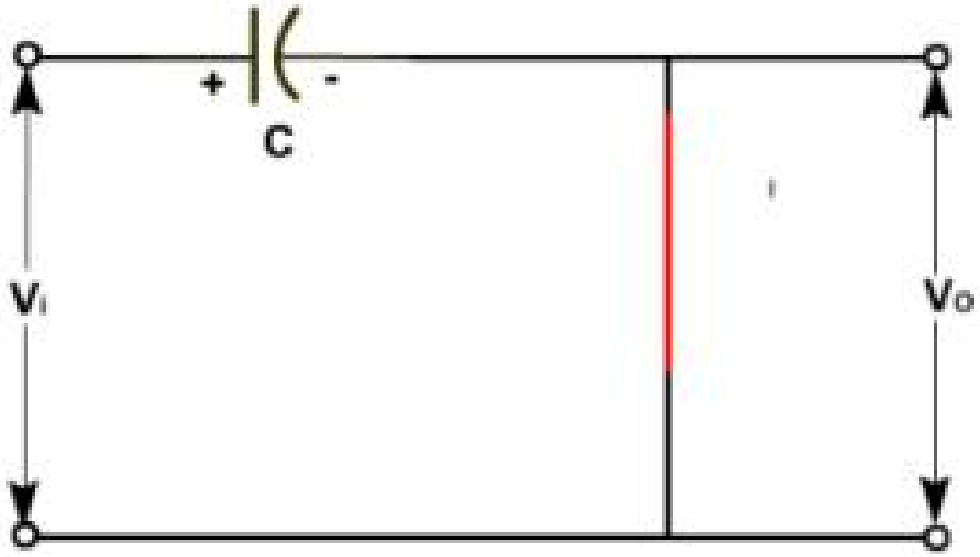
Negative Clamper

Negative clamping circuit clamps the input signal to the -ve Dc level i.e. below the zero level.



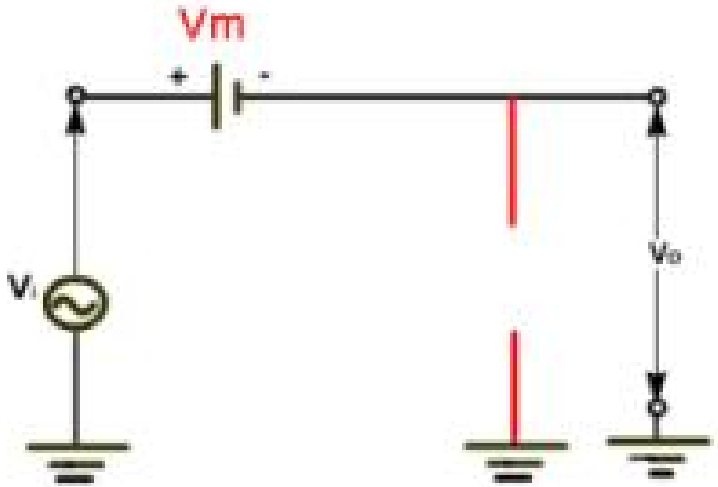
Negative Clamper : +ve Half Cycle

During the positive half cycle the diode conducts and acts like a short circuit. The capacitor charges to peak value of input voltage V_m. During this interval the output Vo which is taken across the short circuit will be zero .



Negative Clamper : -ve Half Cycle

During the negative half of the input signal, the diode does not conduct and acts as an open circuit.

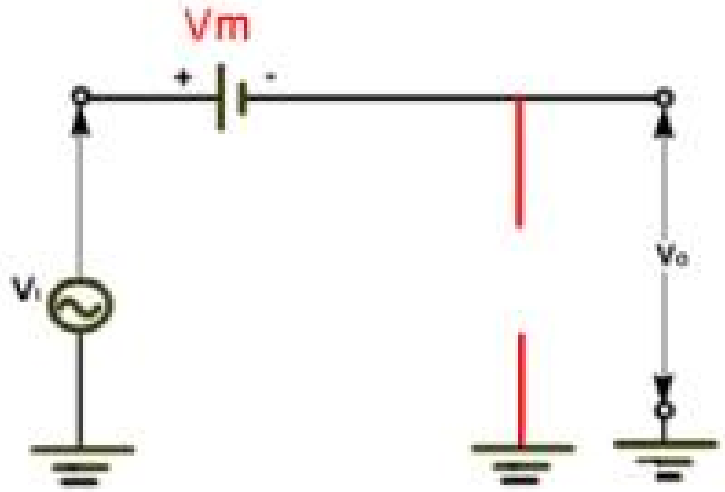


Negative Clamper – Circuit Analysis

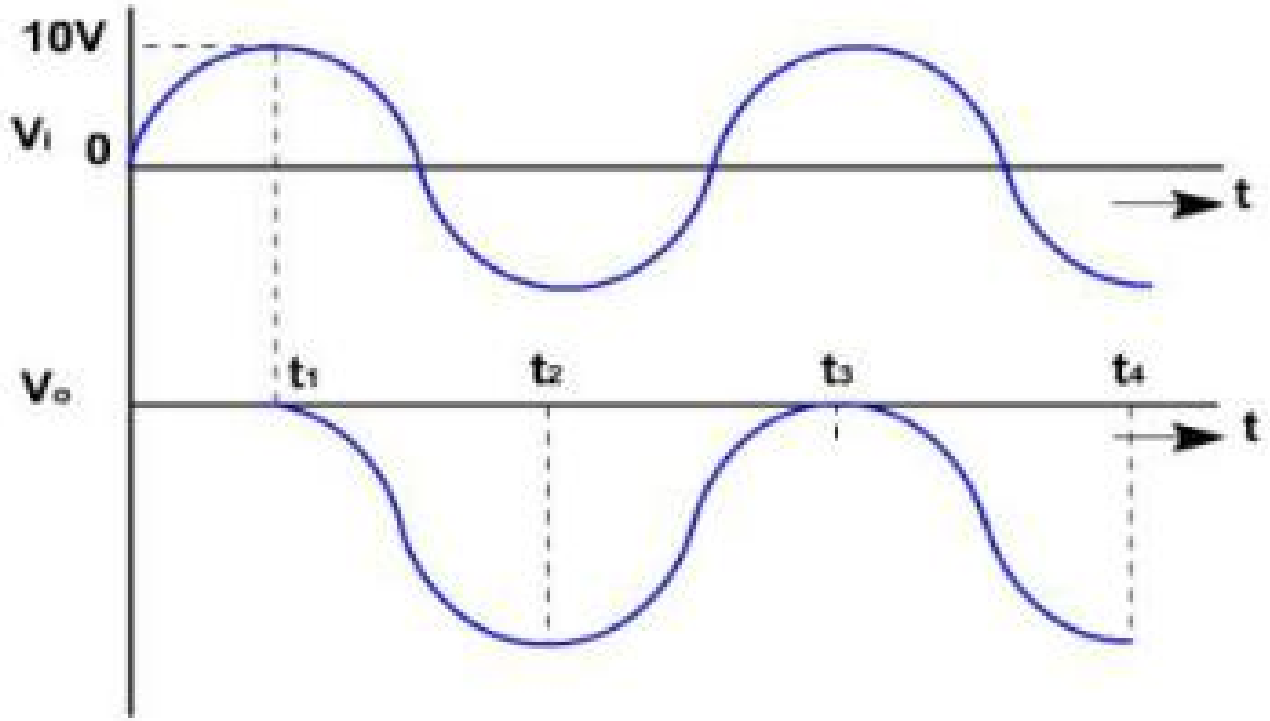
The output voltage can be found by applying KVL (KVL at maximum negative input, $v_{in}=-V_m$).

$Vm - Vm - Vo = 0$

$Vo = -2\,Vm$

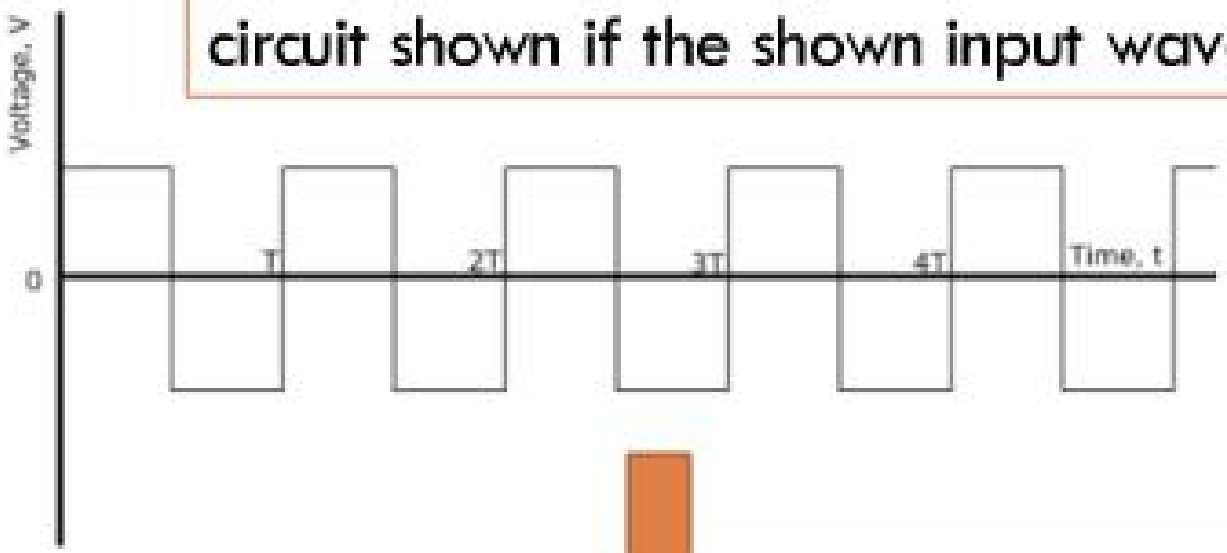


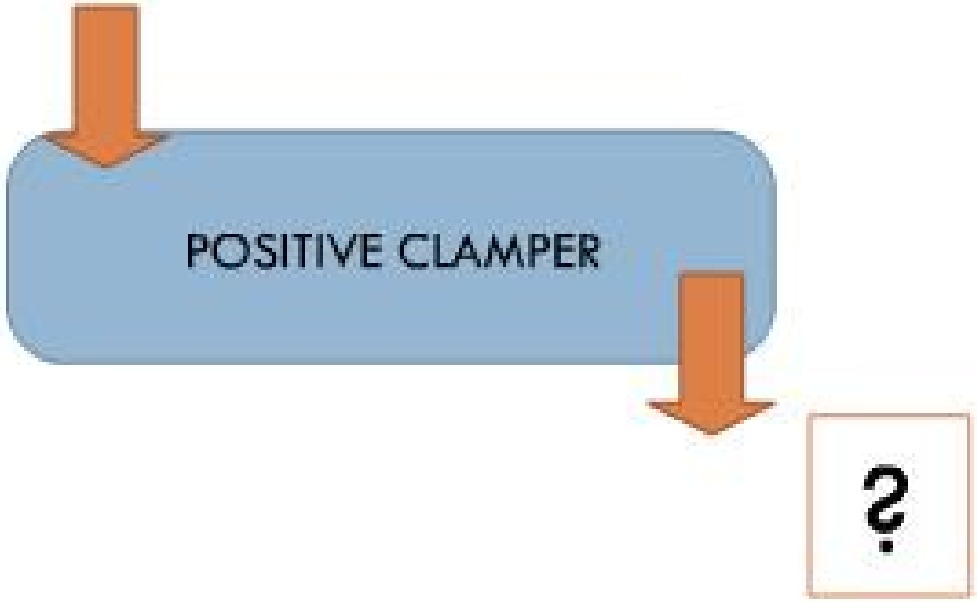
Negative Clamper – Waveform



Exploratory Test

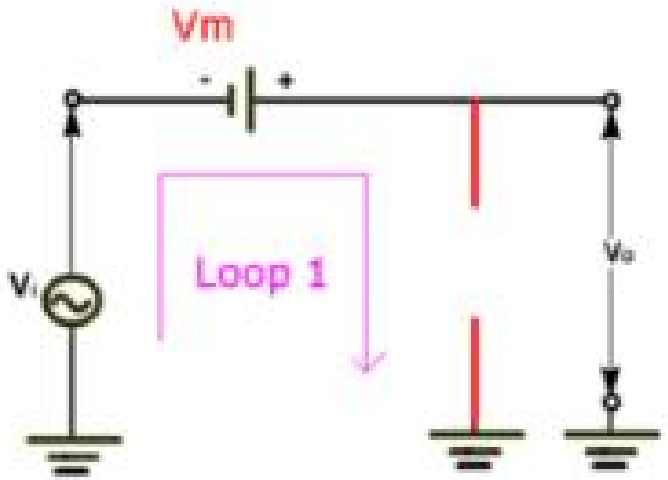
What will be the output of the POSITIVE Clamper circuit shown if the shown input waveform is given ?





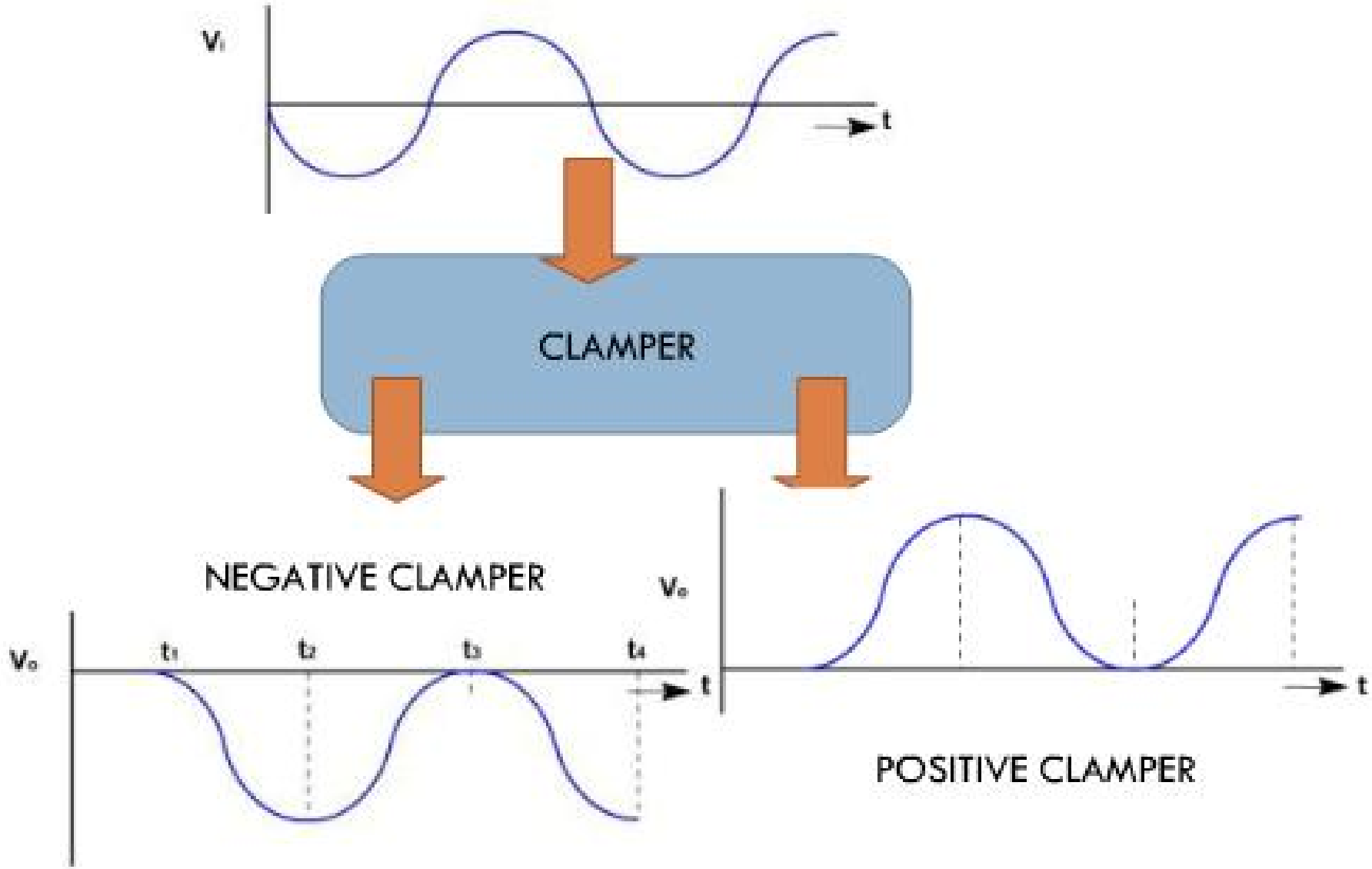
Exploratory Test

During the positive half of the input signal, the diode does not conduct and acts as an open circuit. Capacitor can only discharge through the R(Load). If the Load resistance is small– such that Time constant = 2 * time period of input waveform. How will the output waveform look like ?

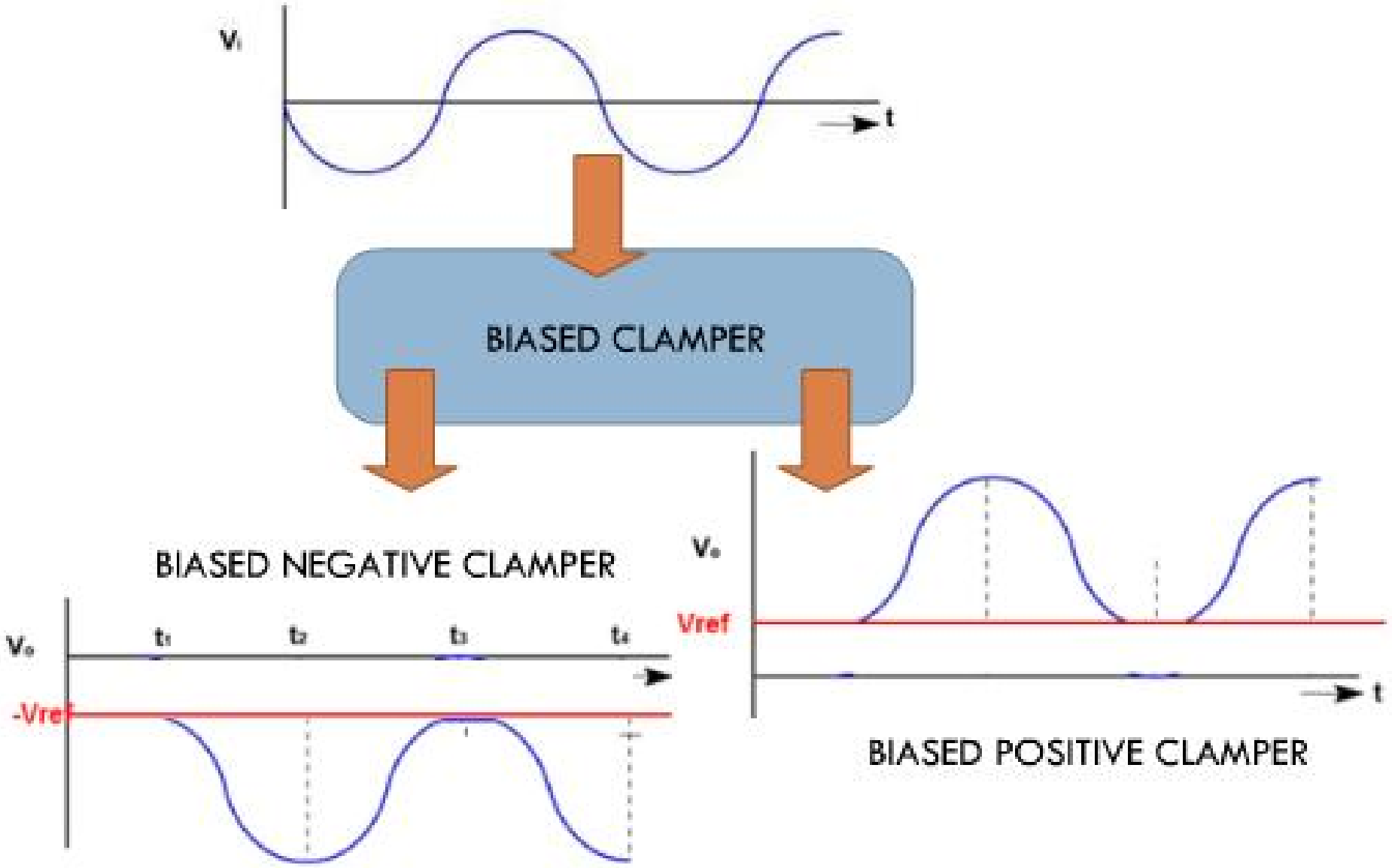


During the + ve cycle diode turns off

Biased Clampers – Until Now



Biased Clampers – Add a higher DC



Biased Clamper

A **biased clamper** allows a waveform to be shifted above (or below) a dc reference other than 0 V. By using a voltage source and resistor, the clamper can be biased to bind the output voltage to a different value. The voltage supplied to the resistor will be equal to the offset from 0.7V (assuming an Si diode) in the case of either a positive or negative clamper - the clamper type will determine the direction of the offset.