COAVL: A Virtual Lab on Computer Organization and Architecture

Chittaranjan Mandal with Gargi Roy and Devleena Ghosh Presenter: Partha De

Dept of Computer Sc & Engg IIT Kharagpur

> COAVL Presentation February 27, 2015

Virtual lab objective and relevance

- COA is a core course in the curriculum of CSE, EE and ECE
- Laboratory experiments essential to understanding basics
- Most places used bread board based setup

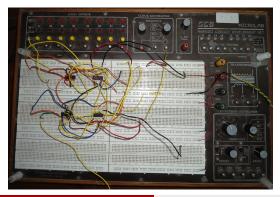
Drawbacks

- Limits the size and extent of experiments
- 2 Time consuming



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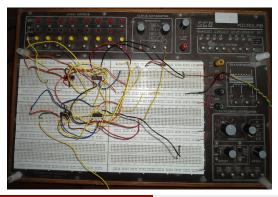
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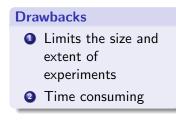
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Virtual lab objective and relevance contd..

- FPGA based lab to overcome this limitation
- Also has some limitations:
 - Learning curve with FPGAs somewhat high
 - Expensive
 - Logistics barrier of running lab
- Hence virtual lab, especially for most institutions

Experiments designed using concept hierarchy

Computer Arithmetic related

- Design of a Ripple Carry Adder
- Design of a Carry-Look-Ahead Adder
- Design of Wallace Tree Adder
- Synthesis of flip-flops
- Design of Registers and Counters
- Design of Combinational Multipliers
- Design of Booth's Multiplier
- Design of an ALU

Memory related

- Design of Memory elements
- Design of Associative cache without replacement policy
- Design of Direct Mapped cache without replacement policy

CPU design related

Design of single instruction CPU



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Web interface of COLDVL

- Pedagogic considerations are reflected in web interface
- Web interface includes set of experiments, manual, others

Web interface of each experiment

- Theory
- Objective
 - Guideline to check key behavior of the design
 - Test plan
 - Assignments
- Procedure
- Experimentation platform (generic simulation platform)considered
- Quizzes
- Further reading

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Features of the COAVL simulator

- The simulator supports 5-valued logic [True(T)(wire color: blue) False(F)(wire color: black) High impedence(Z)(wire color: green) Unknown(X)(wire color: maroon) Invalid(I)(wire color: orange)]
- Capable of simulating combinational circuits and synchronous sequential circuits
- Control signal generation from a user given ASM chart
- Bus based design with wired AND operation to CPU design
- Includes a single instruction CPU design with built-in controller
- Saving with Identification to check plagiarism
- Circuit analysis through different wire colors
- Minimal server dependency by having client side simulation

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The simulator has the following:

Graphical editor

- A canvas to design the circuit
- Click and Drop method to add the components
- Different functional buttons like undo/redo, delete, zoom, save/open, print, showing timing diagram etc.

Palette

- Tools like connection, selection, clone
- All types of logic gates and flip-flops
- Inputs including free running clock
- Display units
- Adders, decoders, multiplexers, registers, counters etc.
- Arithmetic logic units, memory elements including cache memory
- Controller
- Other complex components like single instruction CPU, 4 bit address working memory etc.

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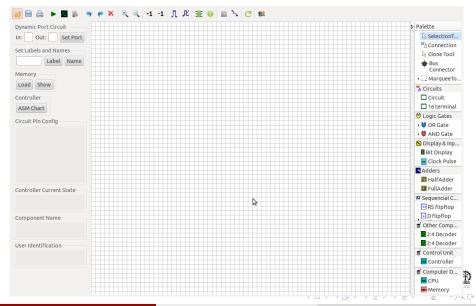
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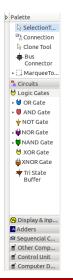
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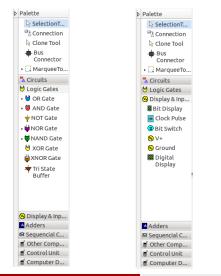
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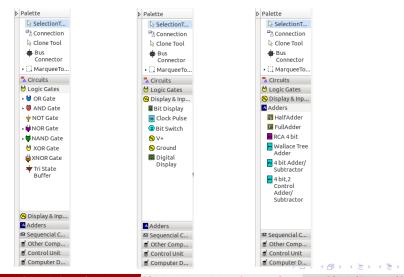


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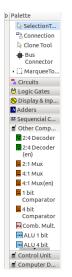


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Component drawers contd..



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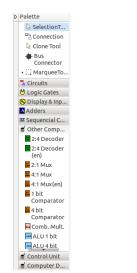
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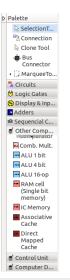
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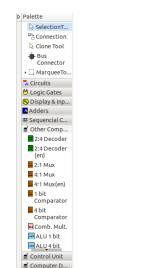


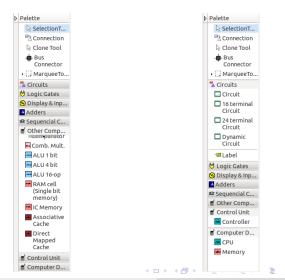


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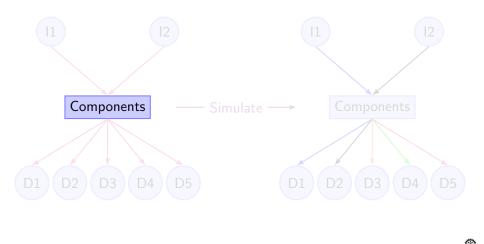


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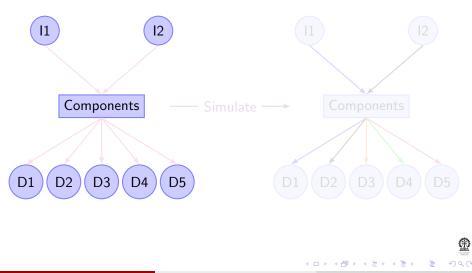




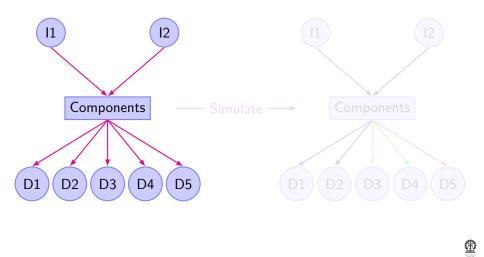
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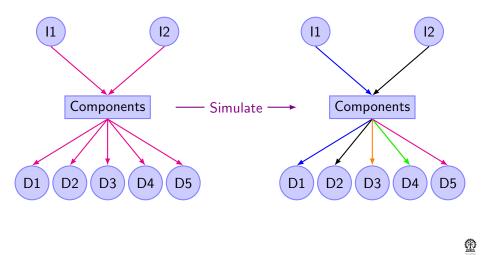
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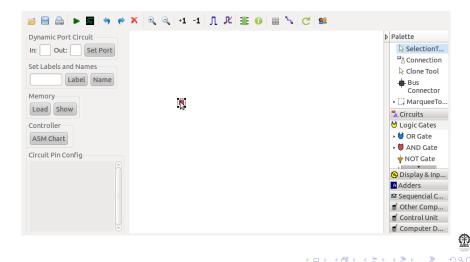
Building a haff adder circuit

To instantiate a component left click on the component icon

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Circuit Pin Config	Not cate Creates a ga Opis can perform Add Opgrat AND Add operation B Sequencial C
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Instantiating a component contd..

Drop the component at desired position



Connecting components

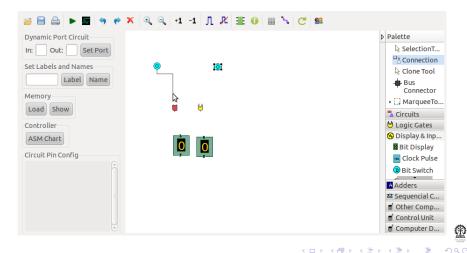
left click on the connection tool

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ASM Chart		😔 Display & Inp
Circuit Pin Config		🛿 Bit Display
		Clock Pulse
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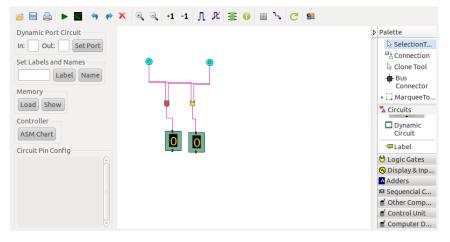
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Connecting components contd..

left click on the output terminal, move the mouse to the desired input terminal



Haff adder circuit



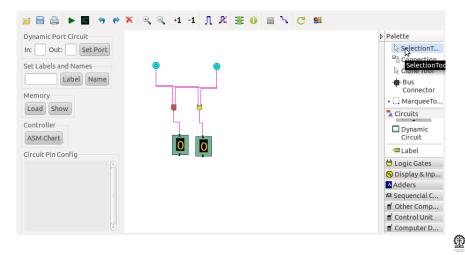


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Clonning components

left click on the selection tool

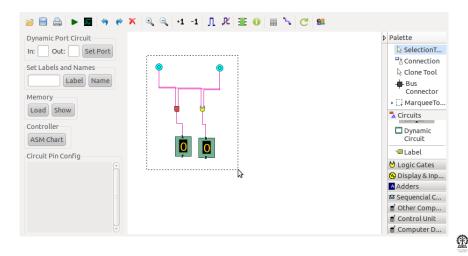


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Clonning components contd..

Select the desired components to be clonned



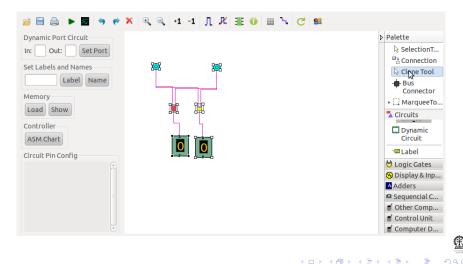
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Clonning components contd..

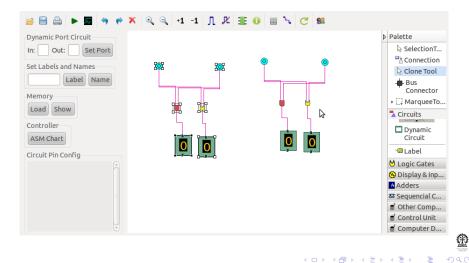
left click on the clone tool





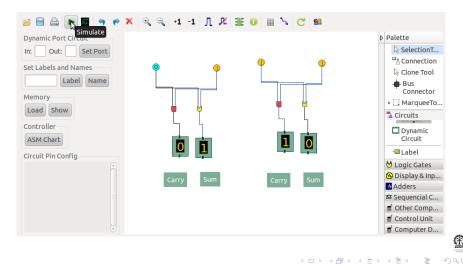
Clonning components contd..

Drag from any selected component



Simulating circuits

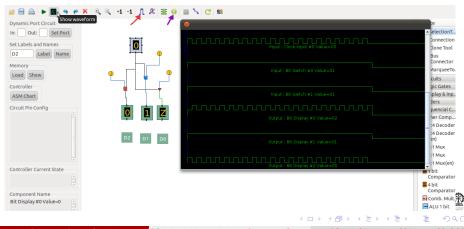
Click on the Simulate button in the top toolbar



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Clock waveform

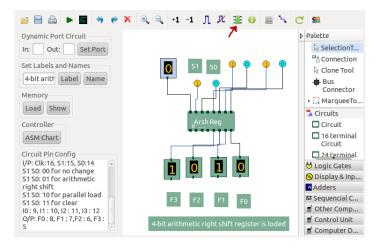
- Click the Show waveform button to see the waveform
- 2 Red arrow indicates the bottun to start the clock
- **③** Violet arrow indicates the bottun to see the component name



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Simulating sequential circuits

Red arrow indicates the bottun to see the pin configuration of a component

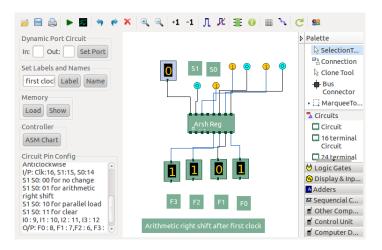




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Simulating sequential circuits contd..



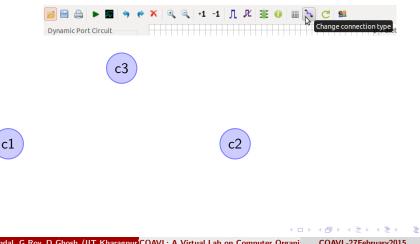


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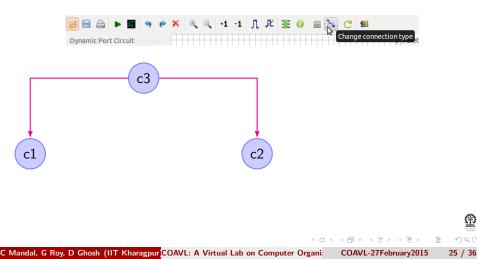
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Change connection type

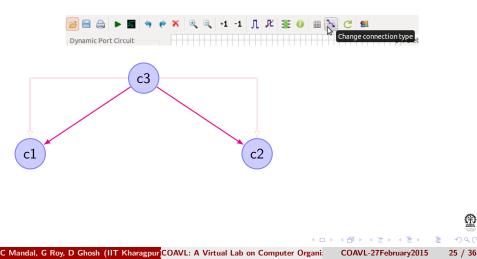


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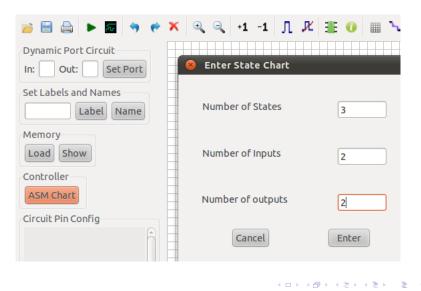
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Generating control sugnals from a given ASM chart



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Generating control sugnals from a given ASM chart contd..

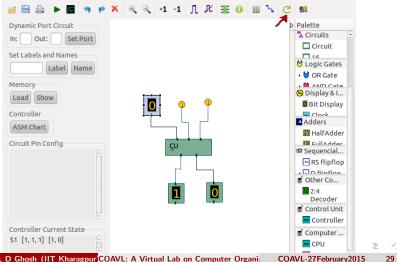
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Dynamic Port Circuit	
In: Out: Set Port	SWT Application
Set Labels and Names	Enter the name of the inputs
Load Show	input1 input2
Controller	
ASM Chart	Enter the name of the outputs
Circuit Pin Config	out1 out2
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Generating control sugnals from a given ASM chart contd..

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Dynamic Port Circuit									
In: Out: Set Port	t 😣 Enter State Table								
Set Labels and Names	_	Inputs Outputs							
Label Name	State	00 01 10 11 out1 out2							
Memory	S 0	S1 • S2 • S0 • S1 • 0 • 1 •							
Load Show	S1	S1 • S2 • S2 • S1 • 1 • 0 •							
Controller ASM Chart	S2	S2 v S2 v S2 v S0 v 0 v 1 v							
Circuit Pin Config	-	Enter							

Generating control sugnals from a given ASM chart contd..

Red arrow indicates the bottun to reset the controller



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Loading working memory to examine the behavior of the single instruction CPU component

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Dynamic Port Circuit	😣 Load	Memory	y Contents							
In: Out: Set Port	Address	MSB	LSB			A	Address	MSB	LSB	
Set Labels and Names	0000						1000			
Memory	0001						1001			
Load Show	0010						1010			
Controller	0011						1011			
ASM Chart	0100						1100			
Circuit Pin Config	0101						1101			
Â	0110						1110			
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: 		L	oad Memor	y		Reset Me	mory		Load from file	
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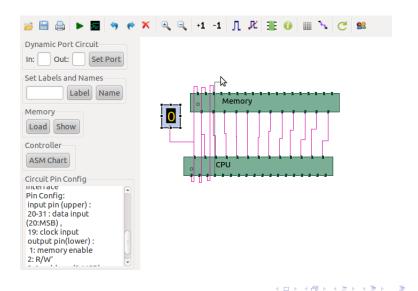
Showing working memory content at any point of time

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Dynamic Port Circui	😣 Mem	ory Conter	ıts.	_	_	_		_	
In: Out: S	Address	MSB	LSB				Address	MSB	LSB
Set Labels and Name	0000	10100010	10001				1000	00000	0000000
Label	0001	1000000	00000				1001	00000	0000000
Memory Load Show	0010	0000000	00000				1010	00000	0000000
Controller	0011	00000000	00000				1011	00000	00000000
ASM Chart	0100	00000000	000010				1100	00000	00000000
Circuit Pin Config	0101	0000000	000101				1101	00000	00000000
	0110	0000000	00000				1110	00000	00000000
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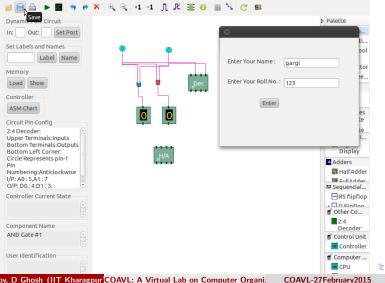
Connecting the CPU with working memory



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Saving components with identification

Click the save button



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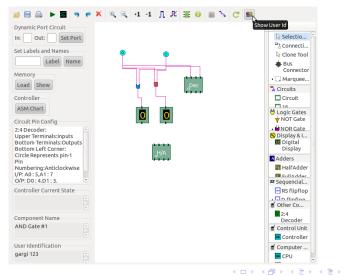
Saving components with identification contd..

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Saving components with identification contd..

Click the Show User Id button to see identification in a saved file



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Thank you!



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